REMARKS

Claims 1-11, 49 and 50 stand rejected under 35 U.S.C. § 112, first paragraph (enablement) and under 35 U.S.C. § 103 over Christie et al. '975. In order to expedite prosecution, claim 1 has been canceled so as to render the rejections thereto moot. Claims 49 and 50, as amended, and new claim 51 are believed to be patentable over the cited prior art.

On page 3, line 7 of the outstanding Office Action, the Examiner asserts that "0 is included in the claim limitation." Accordingly, to overcome this interpretation, claims 49-51 recite a "natural number".

On page 5, lines 5-7 from the bottom of the outstanding Office Action, the Examiner asserts that "it is known in the art that a circuit element such as counter or adder has carry logics propagating through its bits. An increasing of bit numbers must account for timing analysis." Although the Examiner may be correct in this respect, it is respectfully submitted that those skilled in the art can readily understand that a counter may be implemented using ROM rather than a logical circuit. By doing so, problems that may arise regarding the timing analysis are sufficiently avoided. On page 5, last line – page 6, line 2 of the outstanding Office Action, the Examiner further asserts that "the specification, discusses a hardware element of 3-bit counter to position a packet of processing target instructions. The claims recite an arbitrary number m in which skills in the art shows hardly to implement." However, the following description is found in the specification of the present application at page 45, lines 2 – 16:

> ··· when the number of instruction units in an instruction packet is not a power of 2 ···, in the present embodiment, the position of an instruction unit in an instruction packet is expressed using m different values. By using a calculation that cycles through these m values, the specifying of instruction units and the calculations for shifting the

instruction position can be achieved even if the number of instruction units in an instruction packet is not a power of 2.

As apparent from the above description, the second PC may be any device capable of a calculation cycling through m values. Thus, those skilled in the art can readily understand that the second PC may be implemented using, for example, a state machine, and thus reasonably implementable.

New claim 51 clarifies that an important functionality of the second program counter is "to indicate a position of processing target instruction in the processing packet and sending a carry to the first program counter after indicating every processing target instruction in the packet".

Based on all the foregoing, it is respectfully submitted that claims 1-11 and 49-51 are patentable over the cited prior art.

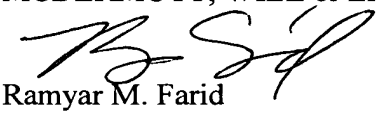
CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 RMF:MWE
Facsimile: (202) 756-8087
Date: March 30, 2004